REMARKS

Claims 1-35 are presently pending in the application. Applicants amend claims 16 and 34, and add new claim 35, as listed above. As discussed in more detail below, support for the amendments and the new claim can be found in the specification. No new matter is added. The application is believed to be in condition for allowance. Hence, reconsideration and allowance are respectfully requested.

Specification

The specification is amended as indicated above to include the serial numbers and/or patent numbers of patent applications listed in the specification to which the present application claims priority.

Claim Objections

Claim 16 is amended as listed above to depend on claim 15, thereby correcting the typographical error regarding the dependency of this claim.

Information Disclosure Statement

In response to the Examiner's request, Applicants herewith provide a legible copy of non U.S. patent references listed in the information disclosure statement (IDS) filed on 7/9/2001.

Rejections Under 35 U.S.C. 102

The Office Action rejects claims 1-34 as being anticipated by U.S. Patent Publication No. 2002/0059424 of Ferguson.

Claim 1 recites a telecommunications network device that includes a plurality of distributed processors. A data path and a switched control path are coupled to the plurality of distributed processors.

The Ferguson patent application was filed on April 24, 2001, and claims priority to provisional application number 60/235,281, filed on September 25, 2000. As discussed in more detail below, the subject matter of claim 1 finds support in several applications filed prior to

September 25, 2000 to which the present application claims priority. Hence, Ferguson is not prior art relative to claim 1.

In particular, the present application is a continuation-in-part of U.S. Patent Application Serial Number 09/663,947 entitled "Network Management System Including Custom Object Collections," filed on September 18, 2000. Support for claim 1 can be found in this patent application, for example, in the passage extending from line 19, page 9 to line 19, page 10 of the specification (a copy of these pages as well as FIGURE 1of the priory document are attached as Exhibit A for the Examiner's convenience). This passage not only describes a distributed processing system comprising a plurality of processors, but it also recites an internal communication bus connected to each processor. The specification further indicates that the communication bus can be a "switched Fast Ethernet providing 100 Mb of dedicated bandwidth to each processor allowing the distributed processors to exchange control information at high frequencies." This passage further recites that in such an embodiment, "Ethernet 32 provides an out-of-band control path, meaning that control information passes over Ethernet 32 but the network data being switched by computer system 10 passes to and from external network connections 31a-31xx over a separate data path." Additional support can be found, e.g., on page 154 of the specification.

Accordingly, claim 1 and claims 2-12, which depend either directly or indirectly on claim 1, are patentable over Ferguson.

Independent claim 13 recites a telecommunications network device having a plurality of distributed processors and a data path coupled to the plurality of the processors. The device further includes a control path having a plurality of control links (e.g., Ethernet ports), wherein at least one of the control links is coupled with each of the plurality of the distributed processors.

The above-described passage of the parent application together with FIGURE 1 of the parent application to which the passage refers provide ample support for claim 13. In particular, this passage and the associated figure teach a distributed processor system having a data path and control path, and a plurality of links (see Ethernet 32 connected to each processor 26a-n in FIG. 1).

Independent claim 15 recites a telecommunications network device having a plurality of distributed processors and a data path coupled to the processors. The network device further includes a control path coupled to the distributed processors, wherein separate control path resources are dedicated to each of the plurality of distributed processors.

The above parent application provides ample support for independent claim 15, as well. In particular, the above-mentioned passage of this parent application not only describes a network device having a plurality of distributed processors coupled to a data path and a control path but also indicates switched Ethernet can provide "dedicated bandwidth" (i.e., a dedicated control path resource) to each processor.

Accordingly, claim 15 and amended claim 16, which now depends on claim 15, are patentable over Ferguson.

Similar arguments apply to establish that the above-mentioned parent application provides support for the subject matter of independent claims 17, 19, 21, 23, 28, 29 and 30. Thus, these claims and the claims depending thereon are patentable over the cited reference.

New Claim

New claim 35 recites a telecommunications network device that comprises a plurality of distributed processors coupled to a data path and a switched control path. The control path provides a dedicated bandwidth to each processor for transmission of control information. At least one of the distributed processors is coupled to the switched control path through *multiple independent ports*.

Support for the above new claim can be found in the original claims (e.g., claims 1 and 11), pages 4 and 324, and the remainder of the specification. Thus, no new matter is added.

Ferguson describes a network apparatus that can include a plurality of Network Processor Modules (NPMs) that connect to one or more Flow Processor Modules (FPMs). The NPMs facilitate the flow of data into and out of the apparatus and the FPMs apply applications and

services to the data flow. The apparatus further includes at least one Control Processor Module (CPM) that processes data flow requests. The CPM connects to the FPMs and NPMs by an Ethernet Control Bus. The embodiment of FIGURE 4 of Ferguson describes a dual redundant architecture having two redundant Ethernet control planes. Each FPM is connected to both control planes.

There is no indication in Ferguson that each FPM is coupled to the Ethernet bus via multiple ports. In the embodiment of FIGURE 4 of Ferguson, each FPM is coupled to two *separate* Ethernet control planes, and *not* to a single control plane via multiple ports. In contrast, claim 35 recites that at least one of the distributed processors is coupled to the switched control plane through multiple independent ports. As Applicants explain, connecting a processor to multiple ports can provide additional Ethernet bandwidth. *See*, e.g., specification, page 324.

Hence, new claim 35 distinguishes patentably over the cited reference.

CONCLUSION

In view of the above amendments and remarks, Applicants respectfully request reconsideration and allowance of the application. Applicants invite the Examiner to call the undersigned at (617) 439-2514 if there are any remaining questions.

Dated: February 8, 2005

Respectfully submitted,

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APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE OF INVENTION:

NETWORK MANAGEMENT SYSTEM INCLUDING CUSTOM OBJECT COLLECTIONS

Inventors:

John Wagner

Kevin D. Snow

and

Darryl Black

SELECTED PAGES OF PRIORITY DOCUMENT

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EXPRESS MAIL LABEL NO.: EL327514223US

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EXHIBIT A

software, standard system services software and modular system services software. Even portions of the kernel may be hot upgraded under certain circumstances. Examples of metadata include, customization text files used by software device drivers; JAVA class files that are dynamically instantiated using reflection; registration and deregistration protocols that enable the addition and deletion of software services without system disruption; and database view definitions that provide many varied views of the logical system model. Each of these and other examples are described below.

The embodiment described below includes a network computer system with a loosely coupled distributed processing system. It should be understood, however, that the computer system could also be a central processing system or a combination of distributed and central processing and either loosely or tightly coupled. In addition, the computer system described below is a network switch for use in, for example, the Internet, wide area networks (WAN) or local area networks (LAN). It should be understood, however, that the modular software architecture can be implemented on any network device (including routers) or other types of computer systems and is not restricted to a network switch.

A distributed processing system is a collection of independent computers that appear to the user of the system as a single computer. Referring to Fig. 1, computer system 10 includes a centralized processor 12 with a control processor subsystem 14 that executes an instance of the kernel 20 including master control programs and server programs to actively control system operation by performing a major portion of the control functions (e.g., booting and system management) for the system. In addition, computer system 10 includes multiple line cards 16a-16n. Each line card includes a control processor subsystem 18a-18n, which runs an instance of the kernel 22a-22n including slave and client programs as well as line card specific software applications. Each control processor subsystem 14, 18a-18n operates in an autonomous fashion but the software presents computer system 10 to the user as a single computer.

Each control processor subsystem includes a processor integrated circuit (chip) 24, 26a-26n, for example, a Motorola 8260 or an Intel Pentium processor. The control processor subsystem also includes a memory subsystem 28, 30a-30n including a combination of non-volatile or persistent (e.g., PROM and flash memory) and volatile (e.g., SRAM and DRAM) memory components. Computer system 10 also includes an internal communication bus 32 connected to each processor 24, 26a-26n. In one embodiment, the communication bus is a switched Fast Ethernet providing 100Mb of dedicated bandwidth to each processor allowing the distributed processors to exchange control information at high frequencies. A backup or redundant Ethernet switch may also be connected to each board such that if the primary Ethernet switch fails, the boards can fail-over to the backup Ethernet switch.

In this example, Ethernet 32 provides an out-of-band control path, meaning that control information passes over Ethernet 32 but the network data being switched by computer system 10 passes to and from external network connections 31a-31xx over a separate data path 34. External network control data is passed from the line cards to the central processor over Ethernet 32. This external network control data is also assigned a high priority when passed over the Ethernet to ensure that it is not dropped during periods of heavy traffic on the Ethernet.

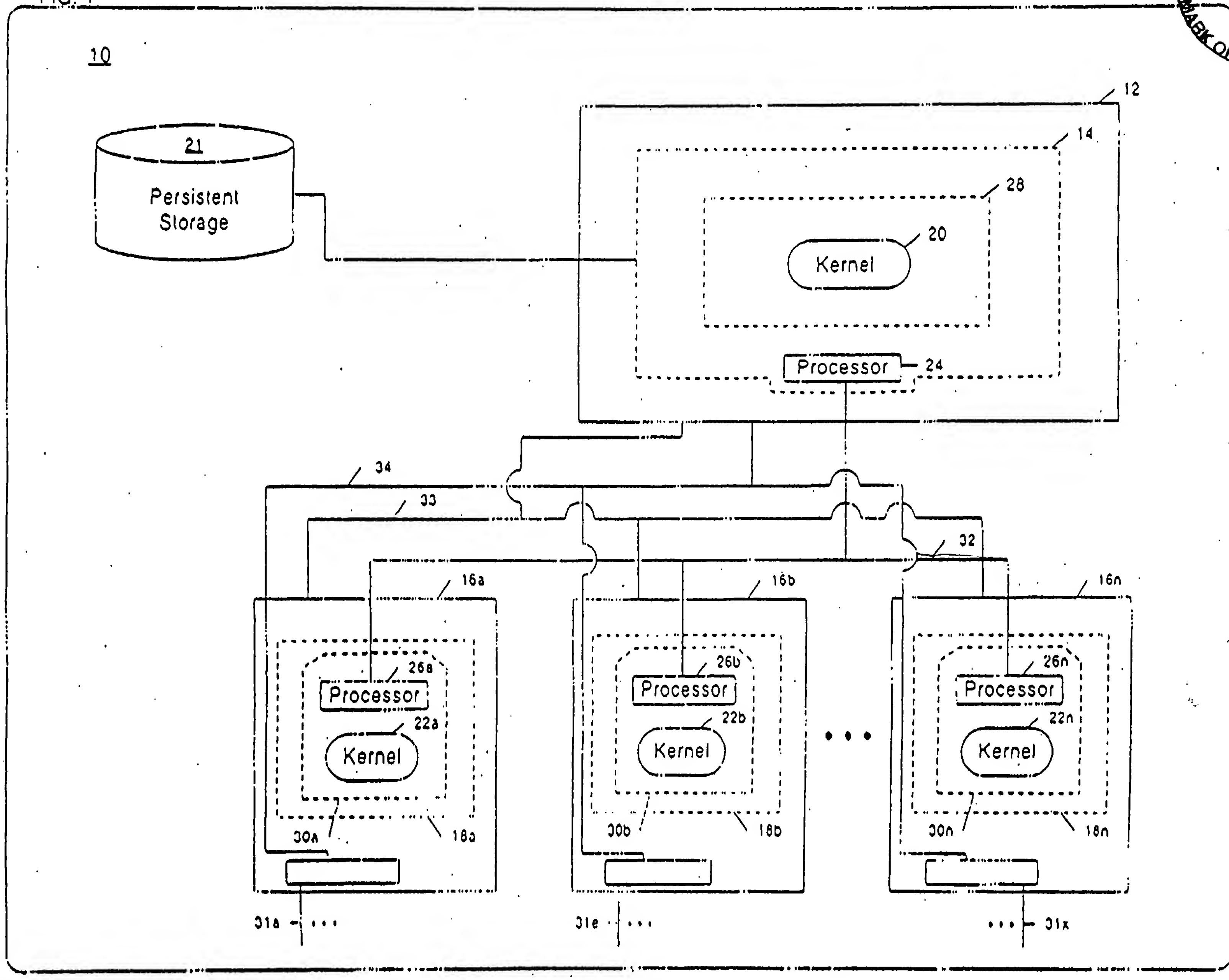
In addition, another bus 33 is provided for low level system service operations, including, for example, the detection of newly installed (or removed) hardware, reset and interrupt control and real time clock (RTC) synchronization across the system. In one embodiment, this is an Inter-IC communications (I^2C) bus.

Alternatively, the control and data may be passed over one common path (in-band).

<u>Network/Element Management System (NMS):</u>

Exponential network growth combined with continuously changing network requirements dictates a need for well thought out network management solutions that can grow and adapt quickly. The present invention provides a massively scalable, highly reliable

FIG. 1


10
21
Persistent Storage
12
14
28
Kernel
20
Processor
24
34
33
32
16a
16b
16n
26a
26b
26n
Processor
Processor
Processor
22a
22b
22n
Kernel
Kernel
Kernel
30a
30b
30n
18a
18b
18n
31a
31e
31x